



35A, 200V N-CHANNEL POWER MOSFET

Features

Advanced process technology

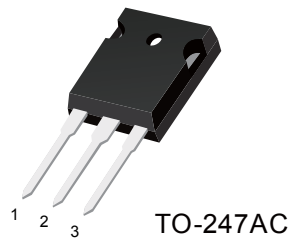
Ultra low On-Resistance

175 °C Operating Temperature

Fast Switching

Repetitive Avalanche Allowed up to T_{jmax}

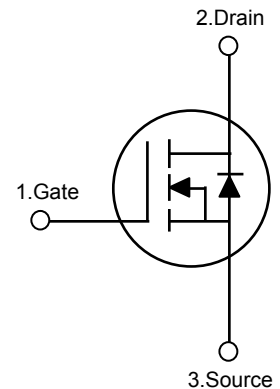
Lead-Free



TO-247AC

Product Summary

V_{DS}	200	V
$R_{DS(ON)}$ Max.	75	m Ω
I_D	35	A



ORDERING INFORMATION

Order Number	Package	Pin Assignment			Packing
		1	2	3	
HPW750N20SPA	TO-247AC	G	D	S	Tube BOX

ABSOLUTE MAXIMUM RATINGS ($T_C=25^\circ\text{C}$, unless otherwise specified)

Parameter	Symbol	Conditions	Value	Unit
Drain source voltage	V_{DS}		200	V
Gate source voltage	V_{GS}		± 20	
Continuous Drain Current	I_D	$T_C=25^\circ\text{C}$	35	A
		$T_C=100^\circ\text{C}$	21	
Pulsed Drain Current	$I_{D,pulse}$	$T_C=25^\circ\text{C}$	140	
Avalanche Current	I_{AS}		35	
Avalanche energy, single pulse	E_{AS}	$I_D=1\text{AS}, V_{DD}=50\text{V}$	600	mJ
Peak Diode Recovery dv/dt	dv/dt		5	V/ μS
Power dissipation	P_D	$T_C=25^\circ\text{C}$	200	W
Linear Derating Factor			1.4	W/ $^\circ\text{C}$
Operating and storage temperature	T_J, T_{stg}		-55 to 150	$^\circ\text{C}$
Soldering Temperature, for 10 seconds		300 (1.6mm from case)		

**Thermal characteristics**

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Thermal resistance, junction-case	R_{thJC}	TO-247AC	--	--	0.66	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thcs}	TO-247AC	0.24	--	--	
SMD Version, Device on PCB	R_{thJA}	TO-247AC	--	--	40	
Maximum Lead Temperature For Soldering Purpose	T_l	TO-248AC	--	--	300	°C

Electrical characteristics, at=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	200	--	--	V
Gate source voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2.0	--	4.0	
Zero gate voltage drian current	I_{DSS}	$V_{DS}=200V, V_{GS}=0V, T_J=25^\circ C$	--	0.1	1	μA
		$V_{DS}=200V, V_{GS}=0V, T_J=125^\circ C$	--	1	100	
Gate-source leakage current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$	--	± 10	± 100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=18A$	--	70	75	m Ω
Gate Resistance	R_G		--	1.9	--	Ω
Transconductance	g_{fs}	$ V_{DS} >2 \times I_D \times R_{DS(on)max}$ $I_D=18A$	17	--	--	S

Dynamic Characteristics

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
lutput capacitance	C_{iss}	$V_{GS}=0V$ $V_{DS}=25V$ $f=1MHz$	--	2850	--	pF
Output capacitance	C_{oss}		--	420	--	
Reverse transfer capacitance	C_{rss}		--	120	--	
Turn-on delay time	$t_{d(on)}$	$V_{DS}=100V$ $V_{GS}=10V$ $I_D=18A, R_G=3\Omega$	--	28	--	nS
Risse time	t_r		--	50	--	
Turn-off delay time	$t_{d(off)}$		--	60	--	
Fall time	t_f		--	40	--	

**Gate Charge Characteristics**

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Gate to source charge	Q_{gs}	$V_{DS}=160V$ $I_D=18A$ $V_{GS}=10V$	--	3	3.9	nC
Gate to drain charge	Q_{gd}		--	5.7	8.5	
Gate charge total	Q_g		--	45	17	

Reverse Diode

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Diode continuous forward current	I_S	$T_C=25^\circ C$	--	--	35	A
Diode pulse current	$I_{S,pulse}$	$T_C=25^\circ C$	--	--	140	
Diode forward voltage	V_{SD}	$V_{GS}=0V$ $I_F=35A, T_C=25^\circ C$	--	--	1.4	V
Reverse recovery time	t_{rr}	$V_{GS}=0V, I_S=35A$ $di_F/dt=100A/\mu s$	--	218	--	μs
Reverse recovery charge	Q_{rr}		--	1.91	--	nC



Test Circuits and Waveforms

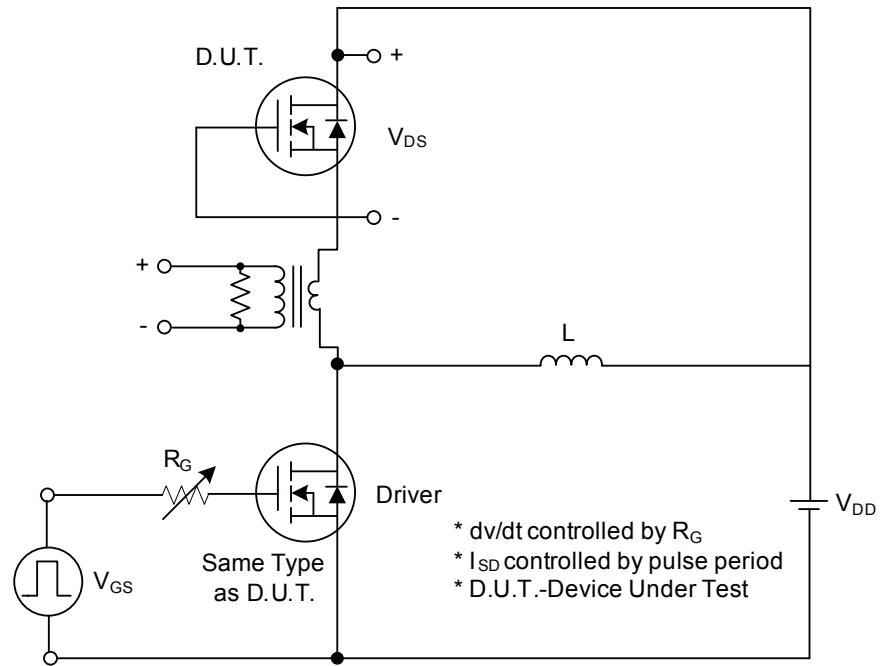


Fig. 1A Peak Diode Recovery dv/dt Test Circuit

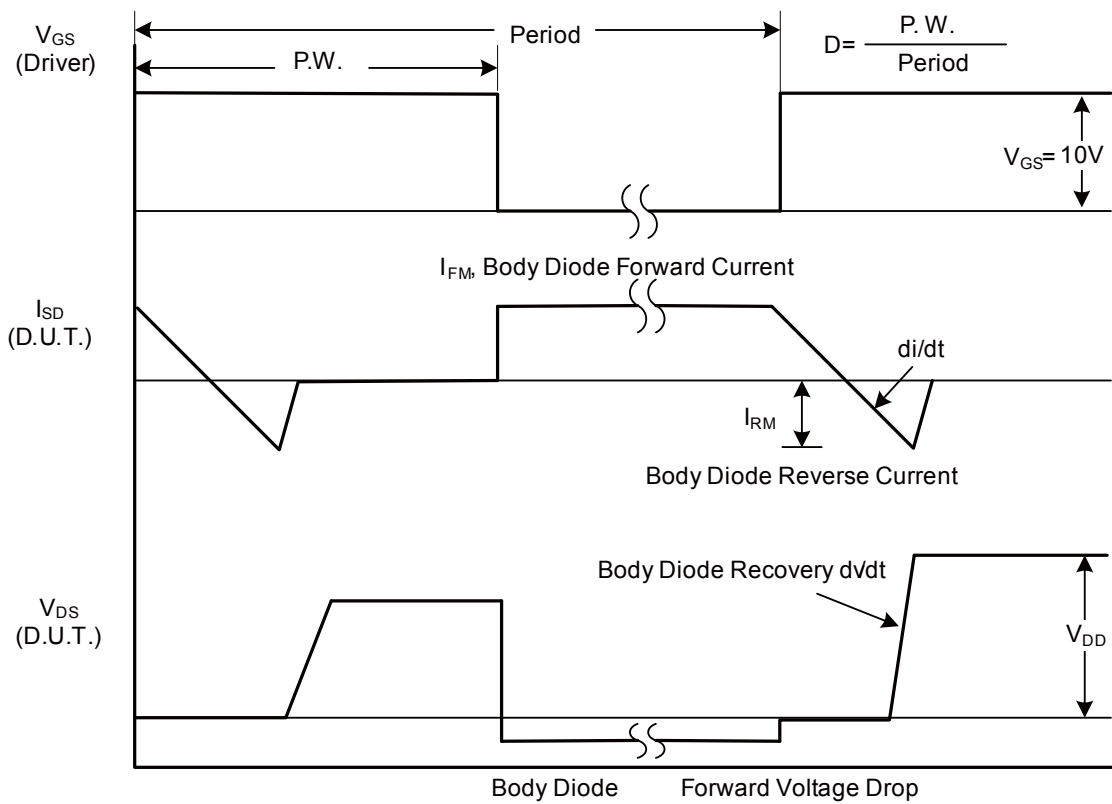


Fig. 1B Peak Diode Recovery dv/dt Waveforms



Test Circuits and Waveforms

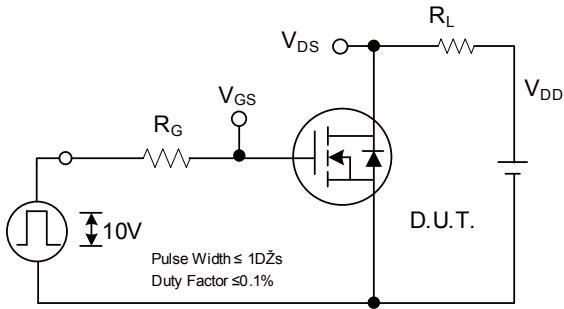


Fig. 2A Switching Test Circuit

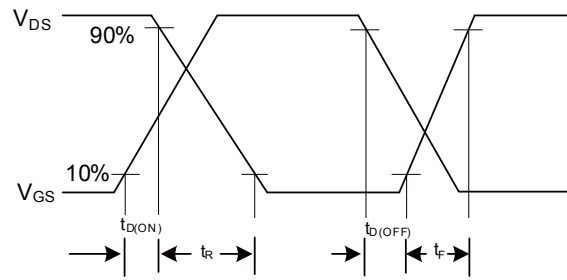


Fig. 2B Switching Waveforms

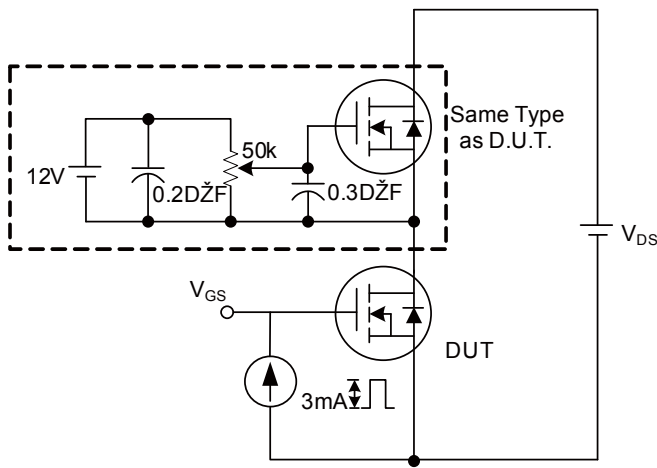


Fig. 3A Gate Charge Test Circuit

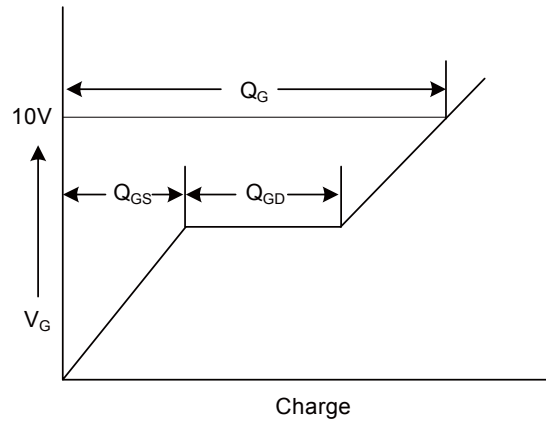


Fig. 3B Gate Charge Waveform

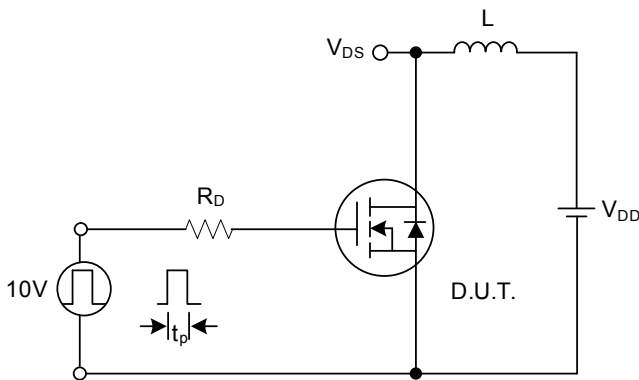


Fig.4A Unclamped Inductive Switching Test Circuit

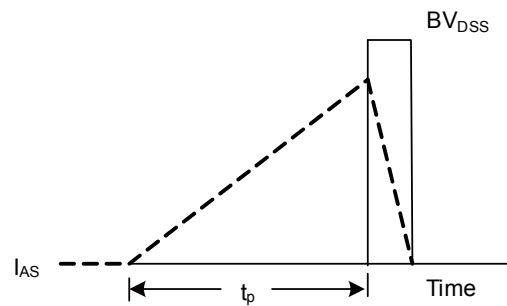


Fig.4B Unclamped Inductive Switching Waveforms

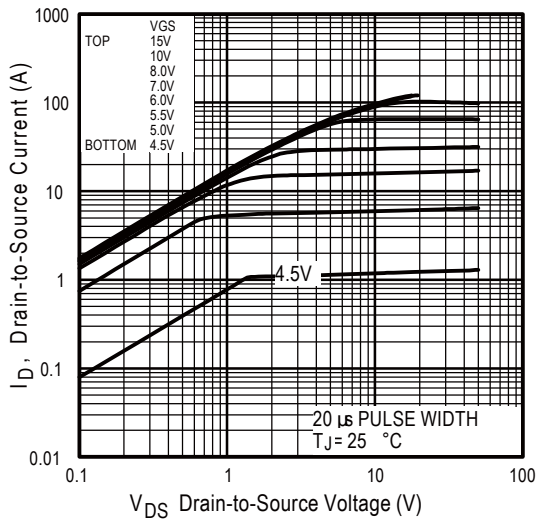


Fig 1. Typical Output Characteristics

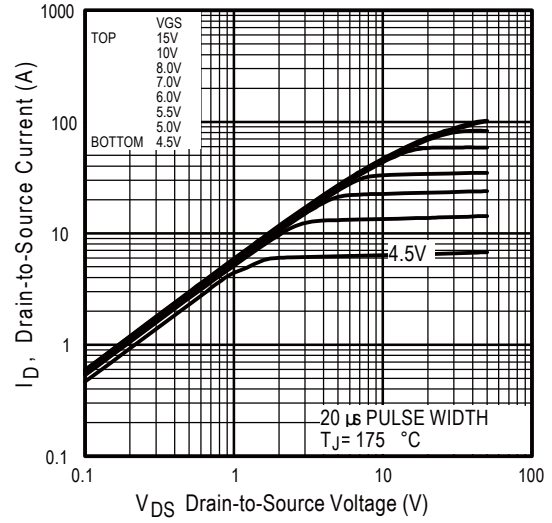


Fig 2. Typical Output Characteristics

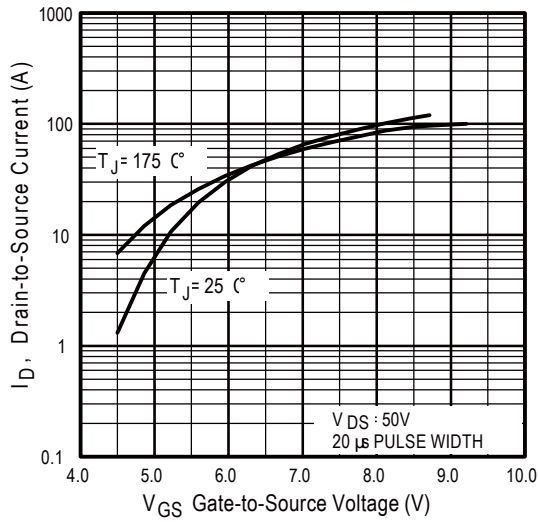


Fig 3. Typical Transfer Characteristics

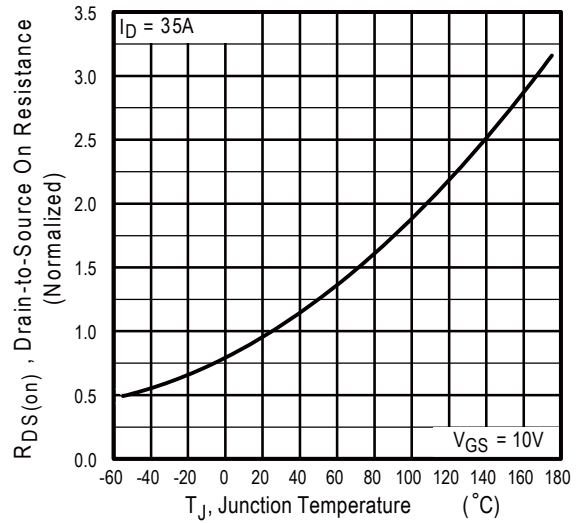


Fig 4. Normalized On-Resistance Vs. Temperature

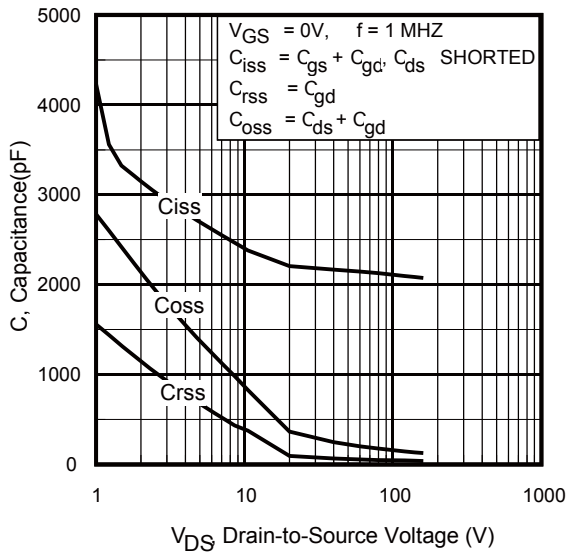


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

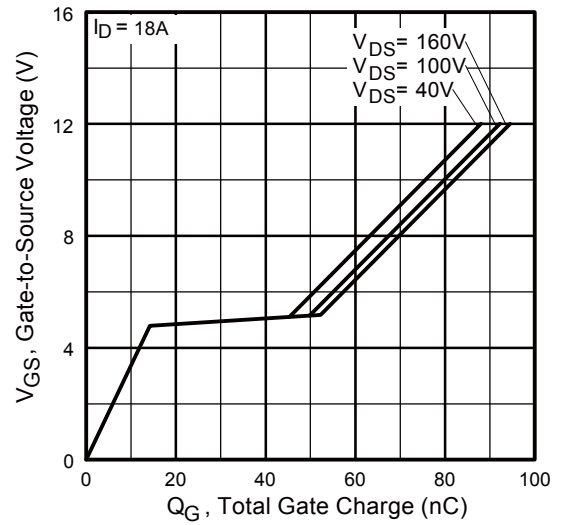


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

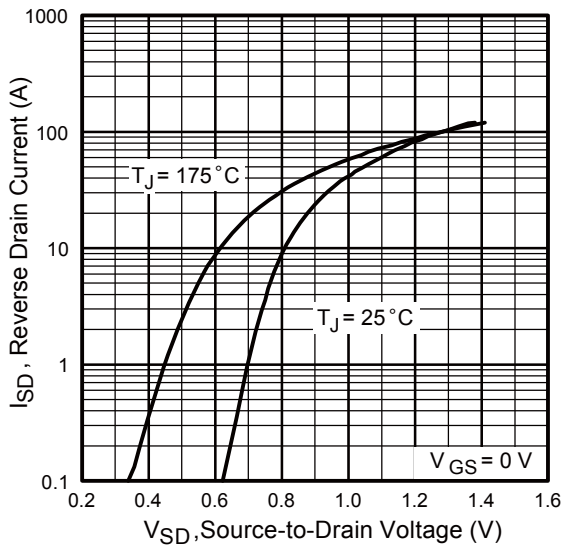


Fig 7. Typical Source-Drain Diode Forward Voltage

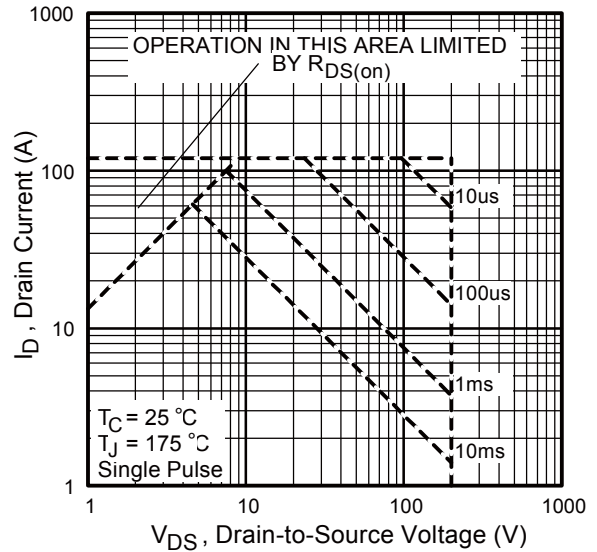


Fig 8. Maximum Safe Operating Area

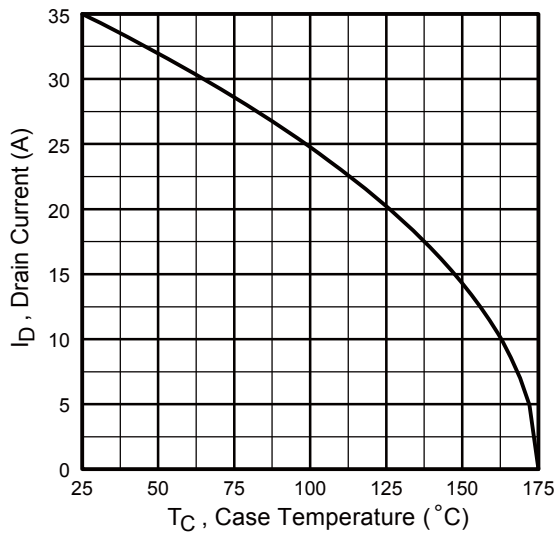


Fig 9. Maximum Drain Current Vs. Case Temperature

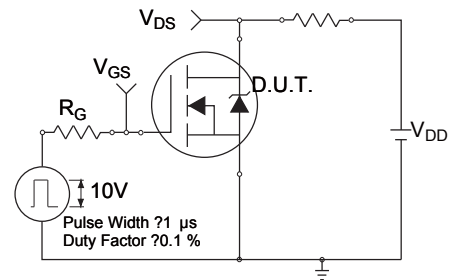


Fig 10a. Switching Time Test Circuit

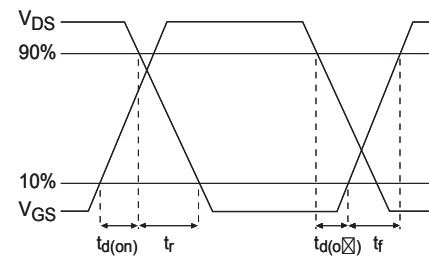
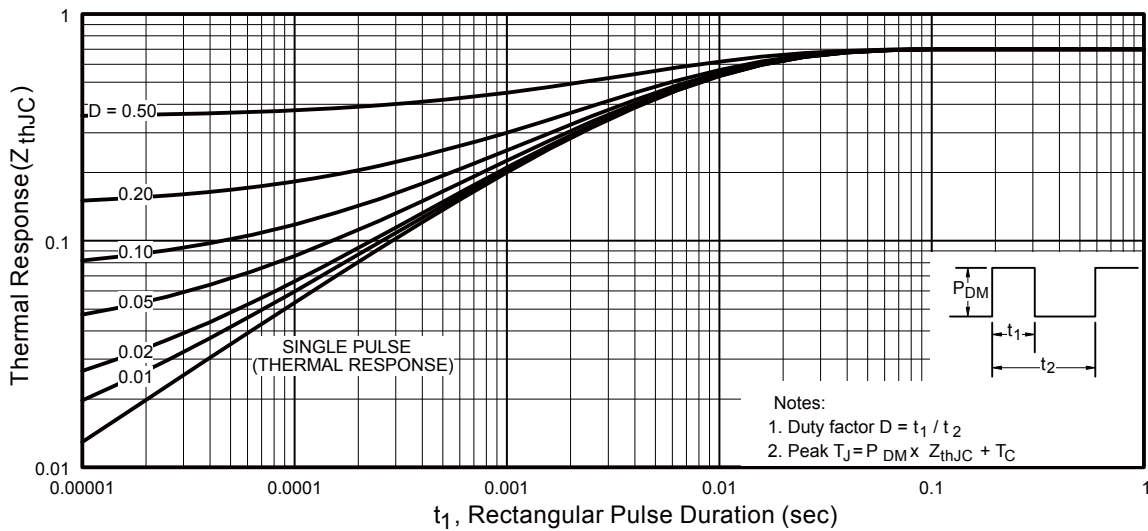


Fig 10b. Switching Time Waveforms





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